

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**  
**APPLICATION FOR U.S. LETTERS PATENT**

Title:

**PROCESS FOR FORMING METALLIZED CONTACTS TO PERIPHERY  
TRANSISTORS**

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## **PROCESS FOR FORMING METALLIZED CONTACTS TO PERIPHERY TRANSISTORS**

### **FIELD OF THE INVENTION**

[0001] The present invention relates to the field of integrated circuits and, in particular, the use of a metal plug structure for contacting doped regions in a periphery transistor of a memory device.

### **BACKGROUND OF THE INVENTION**

[0002] Complex integrated circuits, such as dynamic random access memories (DRAM), have multiple levels of conductors above the surface of a silicon substrate that are used to interconnect various portions of a fabricated circuit.

[0003] For DRAM memory devices, the doped regions or active area of a transistor fabricated in a substrate are typically contacted using polysilicon (poly) plugs, which may connect with a capacitor, a bit line, or other conductor layers. Metal plugs would provide better conductivity than poly plugs; however, metal plugs are typically not used to contact the doped regions of a substrate because of processing restraints including the heat sensitivity of a metal plug to later high temperature fabrication processes and possible active area contamination caused by metal diffusing into the active area of the substrate. For instance, in DRAM memory devices, heat cycles are often used to anneal capacitor structures formed after formulation of the substrate contact plugs, which would melt a metal plug and cause the metal to diffuse into the substrate and thereby contaminate the active area and ruin conductivity between the plug and the substrate. Nevertheless, because of its better conductive properties, it would be preferable if at least some of the conductive plugs to the substrate surface were made of metal instead of polysilicon, particularly for peripheral logic transistors where higher speed operations typically occur.

### BRIEF SUMMARY OF THE INVENTION

[0004] The present invention provides a method and apparatus, which provides an integrated circuit, for example, a DRAM memory device, which utilizes a metal plug structure for contacting doped regions of transistors in the peripheral logic area of the circuitry. The metal plug structure is formed after all high temperature processing steps utilized in wafer fabrication are completed. In particular the invention provides a method for forming metallized contacts to N-channel and P-channel periphery circuit transistor in a memory device by forming the metal plug after a heat cycle process used for capacitor formation and cell poly activation. The metal plugs may be formed prior to forming upper cell plate contacts to the capacitor of a memory device, but subsequent to high temperature processing treatment for the capacitor.

### BRIEF DESCRIPTION OF THE DRAWINGS

[0005] These and other features and advantages of the invention will be better understood from the following detailed description, which is provided in connection with the accompanying drawings.

[0006] FIG. 1 is a cross-sectional view of the early stages of fabrication of a semiconductor device in accordance with an exemplary embodiment of the present invention.

[0007] FIG. 2 shows the semiconductor device of FIG. 1 at a processing step subsequent to that shown in FIG. 1.

[0008] FIG. 3 shows the semiconductor device of FIG. 1 at a processing step subsequent to that shown in FIG. 2.

[0009] FIG. 4 shows the semiconductor device of FIG. 1 at a processing step subsequent to that shown in FIG. 3.

[0010] FIG. 5 shows the semiconductor device of FIG. 1 at a processing step subsequent to that shown in FIG. 4.

[0011] FIG. 6 shows the semiconductor device of FIG. 1 at a processing step subsequent to that shown in FIG. 5.

[0012] FIG. 7 shows the semiconductor device of FIG. 1 at a processing step subsequent to that shown in FIG. 6.

[0013] FIG. 8 shows the semiconductor device of FIG. 1 at a processing step subsequent to that shown in FIG. 7.

[0014] FIG. 9 shows the semiconductor device of FIG. 1 at a processing step subsequent to that shown in FIG. 8.

[0015] FIG. 10 shows the semiconductor device of FIG. 1 at a processing step subsequent to that shown in FIG. 5 according to an alternate embodiment of the present invention.

[0016] FIG. 11 shows the semiconductor device of FIG. 1 at a processing step subsequent to that shown in FIG. 10 according to an alternate embodiment of the present invention.

[0017] FIG. 12 shows the semiconductor device of FIG. 1 at a processing step subsequent to that shown in FIG. 11 according to an alternate embodiment of the present invention.

[0018] FIG. 13 shows the semiconductor device of FIG. 1 at a processing step subsequent to that shown in FIG. 12 according to an alternate embodiment of the present invention.

[0019] FIG. 14 shows the semiconductor device of FIG. 1 at a processing step subsequent to that shown in FIG. 13 according to an alternate embodiment of the present invention.

[0020] FIG. 15 shows the semiconductor device of FIG. 1 at a processing step subsequent to that shown in FIG. 14.

[0021] FIG. 16 is a top down view of a peripheral logic circuitry area of a memory array according to the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

[0022] In the following detailed description, reference is made to various specific embodiments in which the invention may be practiced. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be employed, and that various structural, logical, and electrical changes may be made without departing from the spirit or scope of the invention.

[0023] The term "substrate" used in the following description may include any semiconductor-based structure that has an exposed substrate surface. Structure should be understood to include silicon-on-insulator (SOI), silicon-on-sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. When reference is made to a substrate or wafer in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor or foundation.

[0024] The present invention relates to forming metallized plugs to a substrate, particularly for transistors formed as part of the peripheral logic of a memory device. The present invention will be described as set forth in an exemplary embodiment illustrated below. Other embodiments may be used and structural or logical changes may be made without departing from the spirit or the scope of the present invention.

[0025] In accordance with the present invention, a method is provided for forming metallized plugs for both N and P doped active regions in a peripheral logic

circuitry area, which is typically formed outside of and around the memory cell array area. Referring now to the drawings, where like elements are designated by like reference numerals, FIGS. 1 through 16 illustrate exemplary embodiments of the fabrication steps and resulting structures in accordance with the present invention.

[0026] Referring to FIG. 1, the memory array (indicated generally by reference numeral 100) and the peripheral logic circuit area 200a, 200b are shown during an early stage of fabrication. The peripheral logic circuit area is typically split between an N-channel transistor area 200a and a P-channel transistor area 200b. As shown in FIG. 1, the N-channel transistors in the memory cell array 100 and peripheral logic area 200a, and the P-channel transistor in the peripheral logic area 200b have been formed. The gate stacks in the memory array 100 comprise electrically isolated word lines 112, 113. The gate stacks 15, 16 are associated with respective N-channel and P-channel peripheral logic transistors. Active areas are provided about the gate stacks 12, 13, 15, 16, such as the doped active areas 21, 22, 23, 26, 27, 25, 29, that form Field Effect Transistors (FETs). The memory array includes the gate stacks 11, 12, 13, 14 while the peripheral areas 200a and 200b have respective gate stacks 15, 16. The gate stacks 12, 13 are part of the access transistors 51, 53 for respective memory cells. Each of the gate stacks includes a layer of oxide 120, such as silicon dioxide in contact with the substrate, a conductive gate layer 121 over the oxide, an insulating cap layer 122, and insulating sidewalls 123. The N-channel transistors are formed in a p-well 160 of the substrate while the P-channel transistors are formed in a substrate n-well 161.

[0027] As further shown in FIG. 1, planarized first insulating layer 10, formed of, for example, borophosphosilicate glass (BPSG) or silicon dioxide has been formed over the gate stacks and active areas. The first insulating layer is preferably planarized by chemical mechanical polishing (CMP) or other suitable means. FIG. 1 also shows a pair of gate stacks 11, 14 or for other memory cells in a different cross-sectional plane from that illustrated, which are used for self-aligned

fabrication processes, and first field oxide regions 24 for isolating memory cells in the memory array 100.

[0028] The structure shown in FIG. 1 is conventional but serves as the starting foundation for the invention. The process of the present invention begins by applying a photoresist mask 18 to the first insulating layer 10. Openings 163 in the mask define etch locations and are positioned over the doped active areas 21, 22, 23.

[0029] A first portion of the first insulating layer 10 is next removed by etching to expose the active areas 21, 22, 23 which are N+ doped for the N-channel transistors 51, 53. Plug openings 31, 32, 33 are thus provided, as shown in FIG. 2. It is also possible to dope the areas 21, 22, 23 after the etching operation instead of doping these areas prior to etching.

[0030] A directional etching process such as reactive ion etching (RIE) may be used to etch openings 31, 32, 33 (FIG. 2). The etchant conditions are such that only the insulated layer 10 is etched without any or minimal etching of the active areas 21, 22, 23. The peripheral circuitry areas 200a and 200b are not etched at this time.

[0031] As shown by the structure illustrated in FIG. 3, after openings 31, 32, 33 are etched, the photoresist 18 is removed and openings 31, 32, 33 are filled with an N+ doped polysilicon plug 30. The resulting structure is then planarized by, for example, CMP. The polysilicon plugs 30 may be doped after or during plug deposition and the plugs may be deposited by CVD or other deposition techniques, as known in the art. A second insulating layer 40 of, for example, BPSG is then deposited over the planarized plugs.

[0032] The polysilicon (poly) plugs 30 shown in FIG. 3 can be further identified as poly plugs 41, 43, which will connect with subsequently formed

memory cell capacitors and poly plug 42, which will connect with a subsequently formed bit line.

[0033] Referring now to FIG. 4, a directional etching process through a photoresist mask (not shown), such as RIE, is next used to etch through the second BPSG layer 40 and part of the polysilicon plugs 41, 43 to form capacitor container openings 51, 53.

[0034] Referring now to FIG. 5, after the formation of the capacitor container openings 51, 53 a capacitor structure 45 is formed over the semiconductor device 100. Generally the capacitor structure 45 comprises a conductive bottom layer or plate 55, a dielectric layer 57 over the bottom plate, and a conductive upper plate 50. A barrier layer may also be provided between the bottom plate and the poly plugs 41, 43 to prevent migration of the material forming the bottom plate into the poly plugs 41, 43. The bottom plate 55 of each capacitor structure is formed by depositing a conductive layer within openings 51, 53 and then planarizing the upper surface of the structure to remove any conductor layer material on the upper surface of the structure, leaving the bottom conductive layer only in the openings 51, 53. The bottom conductor plate 55 may be a doped polysilicon layer and may further include an HSG layer. The dielectric layer 57 and the upper capacitor plate 50, as shown in FIG. 5, are blanket deposited in sequence. The upper capacitor plate 50 is a common layer for all capacitors of a memory array. The bottom conductive plate 55, however, is deposited and patterned by planarization to produce individual capacitors 61, 63 over the poly plugs 41, 43.

[0035] The capacitors must be annealed to be effective, which requires a large amount of thermal energy. For instance, heat processing or heat cycles are typically used to activate or effectively conductively dope the lower cell plate when the lower cell plate is polysilicon. Heat processing may also be used to activate or effectively dope and fix pin holes in the dielectric layer in cases where the upper cell plate is made of polysilicon. Accordingly, heat processing may be applied to only the



lower cell plate, or the lower cell plate and dielectric, or to the entire capacitor structure, depending on the materials used to form the capacitor structure. In any event, the invention forms the metallized conductors to the active regions in the substrate after the heat processing is applied.

[0036] In accordance with the invention after the capacitors 61, 63 are heat processed, metal plugs are formed to the N-channel and P-channel transistors in the peripheral logic areas 200a, 200b and to the bit line plug 42.

[0037] As shown in FIG. 6, a directional etching process or other suitable process is used to etch through a photoresist mask 80 and the BPSG layer 40 to define bit line opening 52. A directional etching process or other suitable process also occurs in the peripheral circuitry area 200 to etch through the photoresist mask 80 and BPSG layers 10, 40 to define the peripheral plug openings 55, 56 thereby exposing the active areas 25, 26 for the N-channel and P-channel transistors in the peripheral areas 200a, 200b. The photoresist mask layer 80 is removed after the etching process.

[0038] As shown in FIG. 7, a metal layer 70 is deposited over the memory array 100 and the peripheral circuitry area 200. Accordingly, the metal layer is formed over the exposed outer surfaces of active areas 25, 26, which are P+ doped for the P-channel transistors or N+ doped for N-channel transistors to form metal peripheral plugs 75, 76. The metal layer is further formed over the bit line poly plug 42 to form metal bit line plug 72. Preferably, the metal layer 70 comprises titanium, titanium nitride, tungsten, cobalt, molybdenum or tantalum, but any suitable metal may be used.

[0039] Referring to FIG. 8 the resulting structure is planarized by, for example, CMP. The metal layer 70 and the upper capacitor plate 50 may, for example, be planarized to remove the metal layer 70 and level upper capacitor plate 50 down to at least a thickness of about 500 Angstroms after CMP. In addition, the

dielectric layer 57 and upper cell plate 50 are etched back away from the conductive plugs 72, 75, 76.

[0040] As shown in FIG. 9, a third insulating layer 60, e.g. BPSG layer 60, is deposited over the upper capacitor plate 50. A photoresist layer is then applied and patterned to form etching openings over the metal plugs 72, 75, 76 and a directional etching or other suitable etch process is next performed to etch through the third BPSG layer 60 to expose contact areas of the metal plugs 72, 75, 76. The etchant conditions are such that only the insulated layer 60 is etched without any or minimal etching of the metal plugs 72, 75, 76. The exposed contact areas of the metal plugs 75, 76 in the peripheral areas 200a, 200b are preferably of a smaller surface area than the diameter of the metal plugs 75, 76.

[0041] As further shown in FIG. 9, once the photoresist layer (not shown) is removed, a conductive layer 90 formed from a suitable conductive material such as tungsten or other metal, is deposited over the third BPSG layer 60 to form the contacts 92, 95, 96. The contacts 92, 95, 96 may be of any suitable size and shape so as to provide a low resistance vertical and lateral path to the active areas 22, 25, 26. The contacts 95, 96 in the peripheral areas are preferably of a smaller area than the peripheral metal plugs 75, 76. The peripheral contacts 95, 96 are preferably round in top down cross-sectional shape as shown in FIG. 15, even though the metal plugs 75, 76 have an oval top down cross-sectional shape.

[0042] An alternate embodiment is described with reference to FIGS. 10-15. Like numerals from the first described embodiment are utilized where appropriate, with differences being indicated by 300 series numerals or with different numerals. FIG. 10, shows a processing step conducted subsequent to the processing steps shown in FIG. 5. As shown in FIG. 10, a directional etching process or other suitable process occurs in the peripheral circuitry area 200 to etch through a photoresist mask 380 and the BPSG layers 10, 40 thus forming peripheral plug openings 355, 356 and exposing active areas 25, 26 for the N-channel and P-

channel transistors in the peripheral areas 200a, 200b. The photoresist mask layer 380 is removed after the etching process. Unlike the processing step shown in FIG. 6, the bit line is not etched at this time.

[0043] Referring to FIG. 11, a metal layer 370 is deposited over the memory array 100, and the peripheral circuitry area 200. Accordingly, the metal layer is formed over the exposed outer surfaces of active areas 25, 26, which are P+ doped for the P-channel transistors or N+ doped for the N-channel transistors, to form metal peripheral plugs 375, 376. Preferably, the metal layer 370 comprises titanium, titanium nitride, tungsten, cobalt, molybdenum or tantalum, but any suitable metal may be used.

[0044] As shown in FIG. 12, the metal layer is planarized by, for example CMP. The metal layer 370 may for example be planarized to remove the metal layer 370 and level the upper capacitor plate 50 down to at least a thickness of about 500 Angstroms after CMP. In addition, the dielectric layer 57 and upper cell plate 50 are etched back away from the conductive plugs 375 and 376.

[0045] As shown in FIG. 13, a third insulating layer 360, e.g. BPSG layer 360, has been deposited over the substrate to fill openings around the capacitors 61, 63. A photoresist layer 318 is then applied over the third insulating layer and patterned to form etching openings over the bit line poly plug 42 and the metal peripheral plugs 375, 376.

[0046] As shown in FIG. 14, a directional etching or other suitable etch process is performed to etch through the third BPSG layer 360 to form metal plug contact openings 385, 386 and to etch through the second and third BPSG layers 40, 360 to form the bit line opening 352 so as to expose contact areas of the metal plugs 375, 376 and the bit line poly plug 42. The etchant conditions are such that only the insulated layer 360 is etched without any or minimal etching of the metal plugs 375, 376 and the poly plug 42. The metal plug contact openings 385, 386 are preferably of a smaller diameter than the metal plugs 375, 376.

[0047] As shown in FIG. 15, a conductive layer 90 formed from a suitable conductive material such as tungsten or other metal, is next deposited over the third BPSG layer 360 to fill the metal plug contact openings 385, 386 and the bit line opening 352 so as to form contacts 392, 395, 396. The contacts may be of any suitable size and shape so as to provide a low resistance vertical and lateral path to the active areas 22, 25, 26. The contacts 395, 396 in the periphery are preferably of a smaller cross-sectional top view area than the peripheral metal plugs 375, 376. The peripheral contacts 395, 396 preferably have a round top view cross-sectional shape as shown in FIG. 16, even though the metal plugs 375, 376 may have an oval top view cross-sectional shape.

[0048] In accordance with the present invention the metal periphery plugs are formed after the formation of the capacitors. Preferably the process of forming the metal periphery plugs begins after the completion of all high temperature processing steps utilized in wafer fabrication and after any other temperature changes that affect metal plug formation. Preferably, the process begins after the heat cycles used for cell poly activation and capacitor formation. The metal plugs may be formed prior to forming upper cell plate contacts to the capacitor of the memory device but subsequent to high temperature processing treatment for the capacitor. Furthermore, the present invention is not limited to the illustrated layers. Any suitable number and/or arrangement of conductive and insulating layers may be used without departing from the spirit of the invention.

[0049] FIG. 16 shows a general top down cross-sectional view of a peripheral logic circuitry area of a memory array according to the present invention. The metals plugs in the peripheral circuitry area 200 are shown as oval metal plugs 225, 226, which provide conductivity down to P+ or N+ doped active areas 25, 26 respectively. Three conductive routing channels 214, 216, 218 are shown extending generally lengthwise. Typically, one or more insulating layers overlay and separate the routing channels 214, 216, 218. Beneath, the BPSG layers, other conductive routing channels are formed extending generally widthwise. As shown, the metal

contact 96 provides for an electrical connection to be made between the routing channel 218 and the active area 26. A metal contact 95 provides for an electrical connection to be made between the routing channel 214 and the active area 25.

[0050] One of the advantages of the present invention is the use of metal plugs down to the active areas of the substrate. This provides reduced resistance in making connections between routing channels and the active areas. Accordingly, by providing metal plugs down to the active areas of the substrate in accordance with the present invention electrical connections can be made without bridging, which allows for tighter pitched electrical connections. In addition, by providing oval shaped metal plugs electrical connections can be made to multiple routing channels, as needed.

[0051] The above description and drawings are only to be considered illustrative of exemplary embodiments, which achieve the features and advantages of the present invention. Modification and substitutions to specific process conditions and structures can be made without departing from the spirit and scope of the present invention. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.